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10/619,452	07/16/2003	Yoshiyuki Teshirogi	Q76534	7704

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,452	TESHIROGI ET AL.	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,5,8 and 9* is/are allowed.

6)☒ Claim(s) *1,2,4,7 and 10-14* is/are rejected.

7)☐ Claim(s) *6 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/16/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, March 16th, 2006, the Applicant amended claims 1, 2, 4, 6 and added new claims 7-14. Claims 1-14 are currently pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-2 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. Figures 8-12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 11 is objected to because of the following informalities: claim 11 states, "one of **the** odd numbered bits and one of **the** even numbered bits." It appears the Applicant intended for the above phrase to read, "one of an odd numbered bits and one of an even numbered bits." Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically claim 4 states (at the bottom of page 5), "having a 2^m-bit unit to determine whether $2x2^m$-1-th comparators which are configured to compare." This phrase is seen as vague. Specifically, it is not clear what the "whether" is referring to.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 11-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Specifically, independent claim 11, requires in part for the delay of a single odd and even numbered bit and subsequently the comparison of said delayed odd and even bits with other odd / even bits. The Examiner was unable to locate any enabling discussion within the specification detailing the delaying of odd bits and subsequently using the delayed bits in a comparison operation.

As claims 12-14 depend from claim 11, and inherit all the limitations from claim 11, they are seen as failing to comply with the enablement requirement for the same reasons shown above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (US 6,628,256) in view of Tomiyasu (US 5,712,651).

With respect to claim 1, Nishimura discloses, a video data transfer method of a display device comprising:

determining whether a bit inversion number between first data (dc1 to 24 in fig. 4) and second data (da1 to 24 in fig. 4) following said first data of output video data is more than half or not; and

inverting a logic state of said second data if the bit inversion number is more than half (col. 8, lines 63-67 col. 9, lines 1-5).

Nishimura does not expressly disclose, converting input video data that is composed of parallel data into partially serialized output video data.

Tomiyasu discloses, parallel video data (24 bits (3- 8 bit signals) are input in parallel in fig. 3) that is partially serialized (12 bits (3- 4 bit signals) are output in fig. 3) to be output as video data to a color LCD.

Tomiyasu and Nishimura are analogous art because they are both from the same field of endeavor namely, control circuitry for video data.

At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the partial serialization of Tomiyasu in the inversion detection of Nishimura. This would be accomplished by using Tomyasu's elements 36, 391, 39 of fig. 3 and adjoining them to outputs of Nishimura's fig. 2.

The motivation for doing so would have been to decrease the number of wirings to the signal driver as well as to increase the speed of the data.

Therefore, it would have been obvious to combine Tomiyasu and Nishimura for the benefit of increased data speed to obtain the invention as specified in claim 1.

With respect to claim 2, Nishimura discloses, a video data transfer method comprising:

controlling every $3x2^{(n-m)}$ bits (see 12 in fig. 4, n=4 m=1) a polarity of bits of said input video data that corresponds to said output video data (see dd1to 24 in fig. 4) so that the bit inversion number between first data and second data following said first data of the $3x2^{(n-m)}$-bit parallel of said output video data is $3x2^{(n-m-1)}$ or less (for an example of Nishimura's process see col. 8, lines 62-67 – col. 9, lines 1 –5; states that half of the data ($3x2^{(n-m-1)}$) has to be inverted from previous to subsequent data to trigger the polarity inversion).

Nishimura does not expressly disclose, a video data transfer method of display device comprising:

serializing input video data of a $3x2^n$-bit parallel in a 2^m-bit unit (n and m: natural numbers larger than zero, n>m) to produce output video data of a $3x2^{(n-m)}$-bit parallel.

Tomiyasu discloses, serializing input video data of a $3x2^n$-bit parallel ($3x2^3$-bit input into fig. 3) in a 2^m-bit unit (4-bit unit in fig. 3) (n and m: natural numbers larger than zero, n>m) to produce output video data of a $3x2^{(n-m)}$-bit parallel ($3x2^{(3-1)}$-bit output of fig. 3).

At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the partial serialization means of Tomiyasu (36, 391, 39 in fig. 2) on the output buses of Nishimura (note Nishimura, col. 9, lines 48-57).

The motivation for doing so would have been to decrease the number of wirings to the signal driver as well as to increase the speed of the data.

Therefore, it would have been obvious to combine Tomiyasu and Nishimura for the benefit of increased data speed to obtain the invention as specified in claim 2.

With respect to claim 7, Tomiyasu and Nishimura disclose, the video data transfer method as claimed in claims 1 (see above).

As to the further limitations requiring that the polarity inversion take place prior to the data being partially serialized, the combination of the two pieces of art as described in the above rejection of claim 1 would result in this order of operations.

To further explain, the manipulation of the raw pixel data performed in the color lookup table (fig. 3) of Tomiyasu can be seen as data correction (similar to Nishimura's polarity inversion). The output data from that data correction circuit is in turn partially serialized. It would have been obvious to one of ordinary skill in the art to in turn

perform the partial serialization of data subsequent to the polarity inversion determination of Nishimura.

9. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (US 6,628,256) in view of Wright et al. (US 6,550,026).

With respect to claim 10, Nishimura discloses, a video data transfer method of a display device (fig. 4), the method comprising:

comparing (11 in fig. 4) first data and second data (fig. 4) to output an inversion determination signal (inv2 in fig. 4) if first video data is to be inverted (col. 8, line 62 – col. 9, line 4).

Nishimura does not expressly disclose, comparing individual odd bits with even bits, regardless of whether the odd / even bits are first video data or second video data. Nishimura also doesn't disclose comparing bits of first video data with other bits of first video data.

Wright discloses, comparing odd numbered bits of first video data with even number bits of said first video data (col. 8, lines 45-48).

Wright and Nishimura are analogous art because they are both directed to a similar problem solving area, namely efficient bit data comparison.

At the time of the invention it would have been obvious to one of ordinary skill in the art to compare the odd bits with the even bits as taught by Wright in the data transfer method of Nishimura.

The motivation for doing so would have been, to reduce the number of compare circuits required (Wright; col. 3, lines 33-35).

Therefore it would have been obvious to combine Wright with Nishimura for the benefit of circuitry reduction to obtain the invention as specified in claim 10.

With respect to claim 11, Nishimura discloses, a display control circuit comprising:

a delay circuit (13-1 in fig. 4) which is configured to delay first bits corresponding to one of the odd numbered bits and one of the even numbered bits of video data (input into D) and to output the delayed first bits (Q);

a first comparator (11 in fig. 4) which is configured to compare said delayed first bits and second bits (upper input into 11) corresponding to the other of said odd numbered bits and even numbered bits of the video data.

Nishimura does not expressly disclose, comparing individual odd bits with even bits, regardless of whether the odd / even bits are first video data or second video data. Nishimura also doesn't disclose a second comparator to compare bits of first video data with other bits of first video data.

Wright discloses, comparing odd numbered bits of first video data with even number bits of said first video data (col. 8, lines 45-48).

Wright and Nishimura are analogous art because they are both directed to a similar problem solving area, namely efficient bit data comparison.

At the time of the invention it would have been obvious to one of ordinary skill in the art to compare the odd bits with the even bits as taught by Wright in the data transfer method of Nishimura.

The motivation for doing so would have been, to all an increase in the speed of data comparison (Wright; col. 3, lines 9-12).

Therefore it would have been obvious to combine Wright with Nishimura for the benefit of circuitry reduction to obtain the invention as specified in claim 11.

With respect to claims 12, Nishimura and Wright disclose, the display control circuit as claimed in claim 11 (see above).

Nishimura further discloses, a first control circuit which controls a polarity of said second bits based on the output of said first comparator (12 in fig. 4); and

a second control circuit (10-2 in fig. 2) which controls a polarity of said first bits which are not delayed by said delay circuit based on the output of said second comparator (the inclusion of a second control circuit would have been obvious given the combination of Nishimura and Wright).

10. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (US 6,628,256) in view of Wright et al. (US 6,550,026) and further in view of Tomiyasu (US 5,712,651).

With respect to claims 13 and 14, Nishimura and Wright disclose, the display control circuit as claimed in claim 12 (see above).

Neither Nishimura nor Wright expressly disclose a data parallel to serial converter which is configured to receive the outputs of said first and second control circuits or first and second comparators and to convert parallel video data including said first and second bits to serial video data.

Tomiyasu expressly discloses, a data parallel to serial converter which is configured to receive the outputs of said first and second control circuits (3x8 input bits in fig. 3) and to convert parallel video data including said first and second bits to serial video data (3x4 bit partially serialized data out).

Tomiyasu, Wright and Nishimura are analogous art because they are both from the same field of endeavor namely, control circuitry for data.

At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the partial serialization of Tomiyasu in the inversion detection of Nishimura and Wright. This would be accomplished by using Tomyasu's elements 36, 391, 39 of fig. 3 and adjoining them to outputs of Nishimura's fig. 2.

The motivation for doing so would have been to decrease the number of wirings to the signal driver as well as to increase the speed of the data.

Therefore, it would have been obvious to combine Tomiyasu, Wright and Nishimura for the benefit of increased data speed to obtain the invention as specified in claims 13 and 14.

Allowable Subject Matter

11. Claim 4 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 3, 5 and 8-9 are allowed.

Conclusion

13. The art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoshida et al. (US 6,999,352) discloses a majority decision circuit.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

wlb
8/3/06

AMR A. AWAD
PRIMARY EXAMINER